# Record high-order mode-division-multiplexed transmission on chip using gradient-duty-cycle subwavelength gratings

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**Abstract:** We demonstrate 16-channel mode (de)multiplexers on a silicon chip using gradient-duty-cycle subwavelength gratings. A 1.51-Tbit/s/polarization/wavelength capacity is achieved at 1550 nm with 7 neighboring 50-GHz spaced ASE channels. © 2021 The Authors

## 1. Introduction

Spatial-division multiplexing (SDM) technology has been advancing for several decades, which can be easily combined with wavelength-division multiplexing (WDM) and advanced modulation formats to effectively scale the transmission capacity of an optical communication system. Various studies have been carried out by employing the spatial modes in optical fibers to transmit independent data streams [1]. Recently, silicon-on-insulator (SOI) emerged as a promising platform for high-density integration. On-chip mode-division multiplexing (MDM) has attracted much attention [2] for potential applications in supercomputers and data centers. Mode (de)multiplexers (MUXs) are the key components in MDM systems, capable of combining or separating different mode channels. Conventional mode MUXs are based on asymmetric directional couplers (DCs) [3], which exhibit good scalabilities and compact footprints. However, due to the stringent phase-matching condition, this configuration is highly sensitive to fabrication errors. As a result, most on-chip MDM demonstrations were limited to 5 mode channels on one polarization [4, 5].

To push the limit of mode channels beyond the current status, we proposed a method by introducing a subwavelength grating (SWG)-based DC structure to replace the conventional strip access waveguide in a silicon mode MUX. The two waveguides of the DC can have similar dependences of the mode effective indices on the waveguide widths; thus, the phase matching condition is maintained in the presence of waveguide width variations due to fabrication inaccuracies. An 11-channel mode MUX that supports $TE_0$ ~$TE_{10}$ modes on one polarization was demonstrated [6] on a silicon chip and a high-speed data transmission experiment was carried out with a net capacity of 1.23 Tb/s per wavelength [7]. However, the device performance is dependent on the duty cycles of the SWGs, imposing challenges in fabrication and scalability towards higher order modes.

In this paper, we propose a gradient-duty-cycle SWG (GSWG) structure along the propagation direction of the access waveguide in a DC. The phase matching condition can therefore be maintained for selected waveguide modes over a wide range of coupling positions, thanks to the gradient-duty-cycle structure to achieve the adiabatic process. By using this technique, a record high order mode multiplexing ($TE_0$ ~ $TE_{15}$) is achieved for the first time, to the best of our knowledge. To characterize the performance of the 16-channel MDM device, a transmission experiment is carried out with 112-Gbit/s 16-QAM signals. A multiple-in-multiple-output (MIMO)-based digital signal processing (DSP) algorithm is employed to mitigate the inter-modal crosstalk. The aggregate net data rate can reach a line rate of 28×4×16 = 1792 Gb/s and a net data rate of 1.51 Tbit/s on single polarization/wavelength, which is the highest rate per wavelength on chip. In the experiment, 7 neighboring WDM channels with 50-GHz spacing are loaded with amplified spontaneous emission (ASE) noise, indicating a potential spectral efficiency of 30.2 bit/s/Hz.

## 2. Deign design and operation principle

The schematic configuration of the proposed 16-channel mode MUX is shown in Fig. 1(a). GSWGs are placed along a strip waveguide to construct DCs for the coupling of selected waveguide modes, as shown in Fig. 1(b). A transition taper with a 20-μm length is used to convert the injected $TE_0$ in the silicon nanowire waveguide to a Bloch mode in the GSWG [8]. Note that the duty cycle of the GSWG waveguide is not uniform and transitioned from $\delta$ = 70% to $\delta$ = 30% while maintaining a fixed period value $\Lambda$ = 320 nm. The equivalent material refractive index $n_{eq}$ of the GSWG waveguide can be calculated as [9]:

$$n_{eq}^2 = \delta \cdot n_{Si}^2 + (1-\delta) \cdot n_{Cladding}^2$$

where $n_{Si}$ and $n_{cladding}$ are the refractive indices of the silicon and cladding, respectively. With the introduced gradient duty cycle variation along the propagation direction, $n_{eq}$ of the GSWG waveguide can be transitioned from 3.01 to

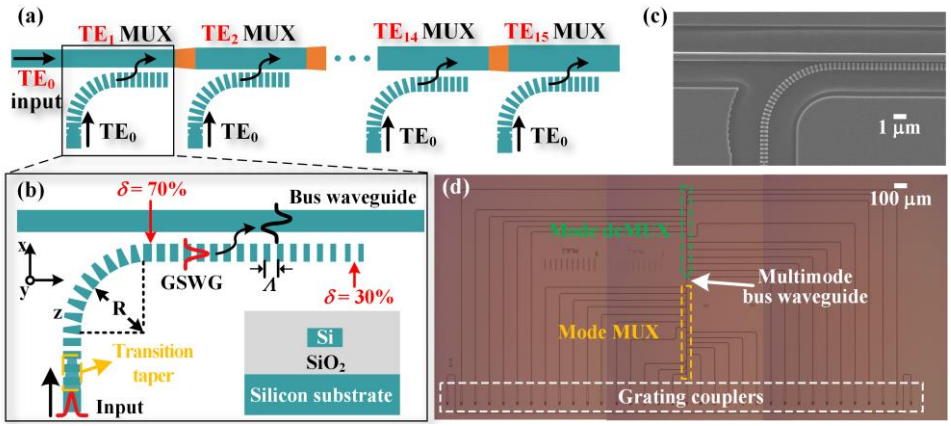


Fig. 1(a) Schematic configuration of the 16-channel mode MUX, (b) illustration of the GSWG-based directional coupler, (c) an SEM image and (d) a microscope image of a fabricated silicon device.

2.25 and a structure with a gradient refractive index distribution can be achieved. It is viable to tune the effective refractive indices of the guided modes in the GSWG waveguides in a wide range to compensate the phase-mismatch of the DCs caused by fabricated deviations, leading to a very-high order mode multiplexing where precise phase-matching condition is required. The structural parameters are calculated to satisfy the phase matching condition of the GSWG-based DC: $n_m = n_{Bloch}$, where $n_m$ and $n_{Bloch}$ are the effective refractive indices of the m-*th* order mode in the bus waveguide and the Bloch mode in the GSWG waveguide, respectively. Note that $n_{Bloch}$ is calculated by using the central duty cycle value of the GSWG waveguide, which is 50% in this case. The calculated bus waveguide widths for $TE_1$ ~ $TE_{15}$ modes are 0.65, 1.01, 1.37, 1.76, 2.09, 2.45. 2.75, 3.14, 3.53, 3.88, 4.22, 4.56, 4.83, 5.17, 5.62 μm, respectively. The gap between the bus waveguide and the GSWG is chosen as 200 nm and the coupling length is 25 μm. An SWG waveguide bend with a 10-μm curvature radius and a trapezoidal segment design is used to sufficiently combine the two waveguides with negligible bending loss [10].

### 3. Device fabrication and characterization

The device was fabricated on a SOI wafer with a 220-nm-thick silicon on top of a 3-μm $SiO_2$ buried oxide. Waveguides and gratings were patterned using electron beam lithography (EBL) and fully etched by inductively coupled plasma (ICP) etching. A 2-μm-thick $SiO_2$ cladding layer was then deposited on top of the devices by plasma-enhanced chemical vapor deposition (PECVD). The microscope image of a fabricated 16-channel mode(de)multiplexer is shown in Fig. 1(d). A 34-channel fiber array is used to couple signals in and out of the

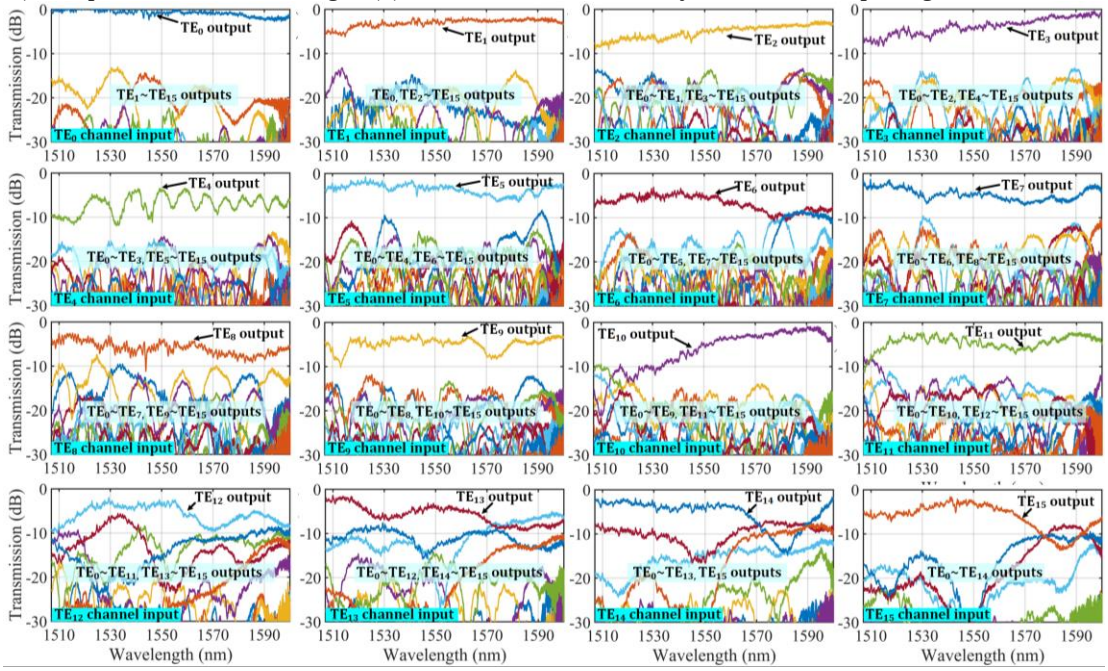


Fig. 2 Measured transmission responses of the 16-channel mode MUX.

silicon chip. Measured transmission results of the fabricated 16-channel mode (de)MUX are provided in Fig. 2. Light is injected from one selected input port and optical signals output from all the 16 output ports are recorded and plotted in Fig. 2. The transmission spectra of the mode (de)MUX are normalized to that of the identical grating couplers fabricated on the same chip with a 6.5 dB/facet coupling loss. Measured insertion losses range from 0.8 dB ~ 5.2 dB and the crosstalk values vary between -9.2 dB ~ -24 dB for all the 16 channels at 1550 nm.

A transmission experiment is conducted to evaluate the performance of the 16-channel MDM device, as shown in Fig. 3. A 64-GSa/s arbitrary waveform generator (AWG) generates a 28-GBaud Nyquist 16-ary quadrature amplitude modulation (16-QAM) signal, which drives a 22-GHz in-phase and quadrature modulator (IQM) biased at the transmission null. The optical 16-QAM signal is amplified and then time gated using an acoustooptic modulator (AOM) with a duty cycle of 12.5%. The time-gated signal is combined with a spectrally shaped ASE noise to emulate 8 WDM channels with a 50-GHz spacing. The WDM signals are then boosted by two erbium-doped fiber amplifiers (EDFAs) before being splitted into 16 channels and injected to the silicon chip. Delay lines are applied to decorrelate the 16-channel signals. At the receiver side, polarization multiplexing and time-division multiplexing are applied before a polarization-diverse coherent receiver. The local oscillator (LO) is also gated and delayed in a similar manner. Due to the relatively large crosstalk of the device, a MIMO-based DSP algorithm is used to recover the 16-QAM data, achieving bit error ratios (BERs) below the 15% forward error correction (FEC) threshold of $1.25\times10^{-2}$ for all the 16 modes [11].

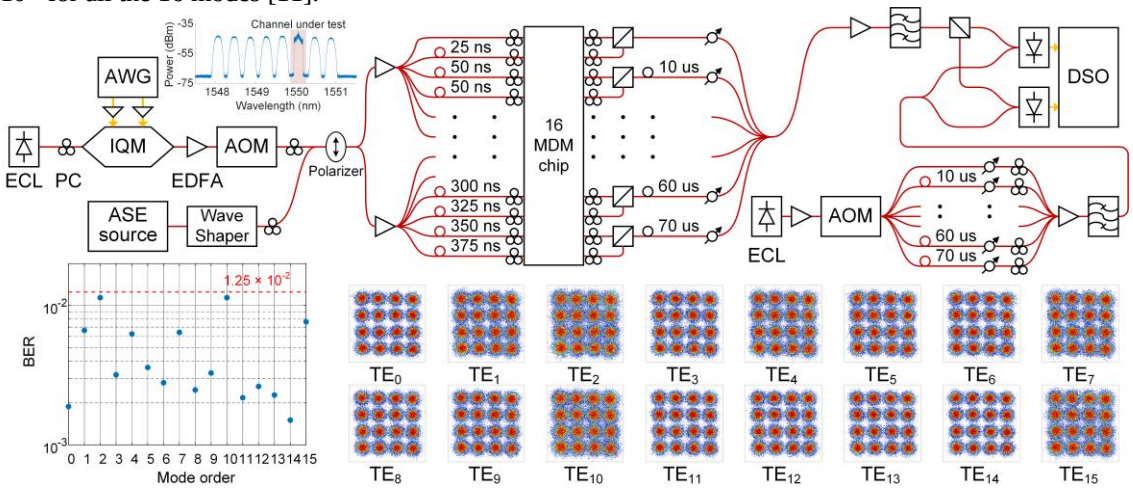


Fig. 3(a) Experimental setup for the MIMO based on-chip 16-mode transmission, (b) calculated BERs and (c) recovered constellation of 28-GBaud 16-QAM signals for 16 modes.

## 4. Conclusion

We demonstrated a 16-channel mode MUX on SOI platform enabled by GSWGs. A record high order mode multiplexing ($TE_0$ ~ $TE_{15}$) on one polarization is achieved. The 16-channel 112-Gbit/s 16-QAM signals are transmitted on chip to achieve a 1.51-Tbit/s/polarization/wavelength capacity at 1550 nm. Seven neighboring 50-GHz spaced WDM channels are loaded with ASE noise, indicating a potential spectral efficiency of 30.2 bit/s/Hz.

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